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<b>**APPLICANTS:</b> Yano Junichi; Yoshida Hisato; Aiba Kimihiko; Imamura Katsuyuki; Mori Junichi; Yamamoto Junya;					
<b>**CONTINUING DATA VERIFIED:</b>					
<b>** FOREIGN APPLICATIONS VERIFIED:</b> JAPAN 2000-371299 12/06/2000					
PG-PUB <input type="checkbox"/> DO NOT PUBLISH <input type="checkbox"/>		RESCIND <input type="checkbox"/>			
Foreign priority claimed <input type="checkbox"/> yes <input type="checkbox"/> no		35 USC 119 conditions met <input type="checkbox"/> yes <input type="checkbox"/> no		ATTORNEY DOCKET NO	
Verified and Acknowledged Examiners's initials		60188-126			
TITLE : Semiconductor integrated circuit					
U.S. DEPT. OF COMM./PAT. & TM-PTO-436L (Rev. 12-94)					

<b>NOTICE OF ALLOWANCE MAILED</b>		Assistant Examiner		<b>CLAIMS ALLOWED</b>	
				Total Claims	Print Claim for O.G.
<b>ISSUE FEE</b>		Primary Examiner		<b>DRAWING</b>	
Amount Due	Date Paid			Sheets Drwg.	Figs. Drwg.
<input type="checkbox"/> <b>TERMINAL DISCLAIMER</b>		<b>PREPARED FOR ISSUE</b>		Application Examiner	
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